DESIGN OF EMBEDDED PASSIVE COMPONENTS IN LOW-TEMPERATURE COFIRED CERAMIC ON METAL (LTCC-M) TECHNOLOGY

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ABSTRACT

This Sarnoff-developed technology combines conventional Low-Temperature Cofired Ceramic technology and a clad Metal base to provide constrained sintering, ruggedness, improved thermal path, and complex cavities with metal ground [1]. *Constrained sintering leads to almost zero shrinkage in the x-y plane during the firing operation allowing the accurate placement of embedded components such as resistors, capacitors, transmission lines, etc.*

This paper describes the development of CAD models for the design and analysis of embedded LTCC-M components. Models were verified by fabricating and testing LTCC-M test coupons for resistors, capacitors, and transmission lines. Results were compared with both EM simulation and circuit modeling. These CAD models operate within the industry standard HP Communications Design Suite utilizing its existing library models [2]; an efficient and cost effective approach. Models, test results, range of validity of these models, and design guidelines will be presented.

INTRODUCTION

Wireless RF products require major performance improvement and size-reduction. Mixed-signal designs tend to use up a large number of passive components. Currently, the vast majority of these products use surface mount discrete parts. The discrete components use a sizable percentage of the printed circuit board area greatly limiting their miniaturization and performance. The component assembly cost is a major constituent of their prices. Embedding passive components during substrate manufacture provides small size, lower cost, better performance, and higher reliability. The 3D integration of all the dc power lines, analog circuits, high-speed digital logic circuits, and RF/microwave components in a multi-layer environment has become the trend and a common target for many of these mixed-signal products.

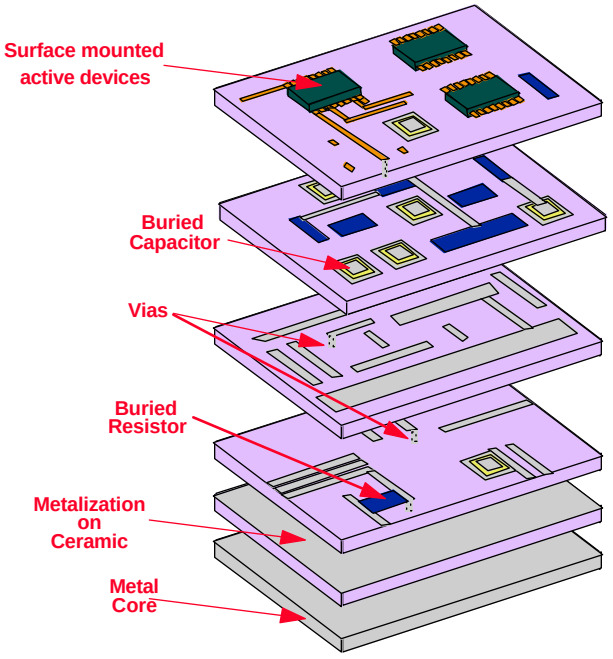

Figure 1 Schematic of a multi-layer LTCC-M circuit showing variuos capabilities

LTCC-M technology allows the manufacture of low-cost 3D circuits using thick-film and cofired ceramic processes. It is enhanced by

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the ability to add embedded passive components (see Fig. 1), offering large scale integration to realize compact size, and lower cost products. The following Tables summarize the features of LTCC-M Technology.

Ideal for high speed digital and mixed signal Applications, and size/cost reduction

Feature	Benefit
Low ε_r increases propagation velocity by 20% vs. Alumina	Shorter propagation delay time
Multi-layer structure	Digital control and analog functions can be supported
Solid ground plane	High isolation/shielding

Ideal for RF/ Microwave and High Power

Features	Benefits
Precision geometry and feature location	Low-Cost replacement for thin film
Low loss, low dielectric constant	Low-Cost microwave feedthru and striplines
Low loss tangent (tan δ < 0.0014) @ 14 GHz	Integrated power combiners
Low-loss silver conductors (<5mΩ)	High-Q impedance matching circuits
Thermal conductivity 170W/m°K; 208 W/m°K spreading, TCE 5.7 ppm/°C (25 to 400 °C)	Performance better than AlN, allows integrated heat sinks, expansion matches Si/GaAs
x-y shrinkage <0.1%	Embedded resistors, capacitors, and vias

The designer must address a new set of questions and issues associated with the implementation of this powerful full-3D technology. Issues include the effect of the LTCC-M surrounding-dielectric on the performance of the embedded components, quality of these components, effect of increased capacitive coupling to ground, the required shielding, via interconnect parasitics, and effects of the neighboring embedded elements. Currently, no commercial CAD models that address these issues are available for embedded structures. EM simulation programs, requiring long execution time, are used to analyze such structures.

This paper presents our successful effort to develop fast and accurate circuit models for LTCC-M embedded components. Circuit models with an adequate degree of accuracy are required for expeditious design cycles for cost-effective and timely manufacture. This is our first step towards generating a complete design kit that will enable the circuit designer to exploit LTCC-M technology to its fullest extent.

CAPACITORS

Embedded capacitors covering the 1pF to few nF range were developed with tight tolerances utilizing different inks. A ± 10% tolerance for the low-dielectric-constant ink (ε_r = 20), and a ± 25% for the high dielectric constant ink (ε_r = 430) have been obtained. Q's of 50 in the 1-2 GHz frequency range were demonstrated.

The semi-distributed circuit parameter model of these embedded capacitors is shown in Fig. 2. It uses components with physical attributes such as width and length; and then all relevant capacitor's dimensions are calculated based on design rules specific to LTCC-M.

Models were verified theoretically and experimentally with excellent agreement. Fig. 3 shows an example of the validation of our circuit model using EM simulation [3]. Good agreement between the circuit model and measured results is demonstrated in Fig. 3. For the high-value dielectric inks, as an example, where circuit model's parameters are based on average measured values of the fabricated capacitance per unit area, circuit models can be closely fitted to the measured results by

optimizing the ink dielectric constant and thickness.

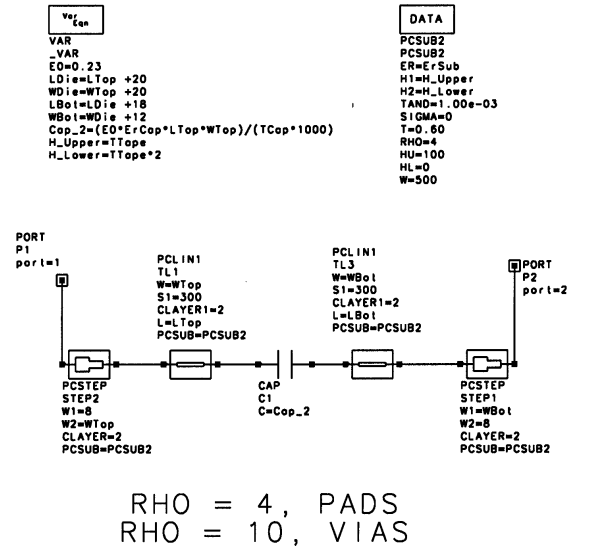

Figure 2 Embedded Capacitor Model

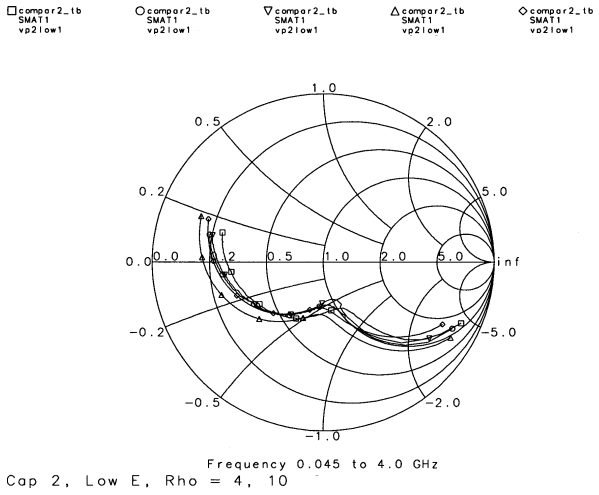

Figure 3 Capacitor Model Validated By EM Simulation and Measurements. Measured results from 3 different boards are represented by: □. ○he▽circuit model is represented by .. The Son△t model is represented by ◇.

RESISTORS

Resistors were fabricated and tested at dc and RF. Resistors within 1/2 to 3 squares and 30-35 mils optimum width can be controlled to within ±15%.

Using the HP Communication Design Suite libraries, an RF circuit model for the buried resistors was developed. The model, shown in Fig. 4, is a distributed parameter model and is based on physical dimensions. The input parameters are: resistor length, width, and dc ink resistivity (Ω/sq.). The number of squares, ink resistivity, and printing dimensions are based on design rules specific to LTCC-M.

This model was validated with EM simulation [3] and compared to measured results for various resistor sizes. Excellent agreement was found between the circuit model (Fig. 5) and measured results. A slight deviation of the measured results in comparison with the model results could be seen especially for the extreme resistor sizes, and can be attributed to screen printing non-uniformity.

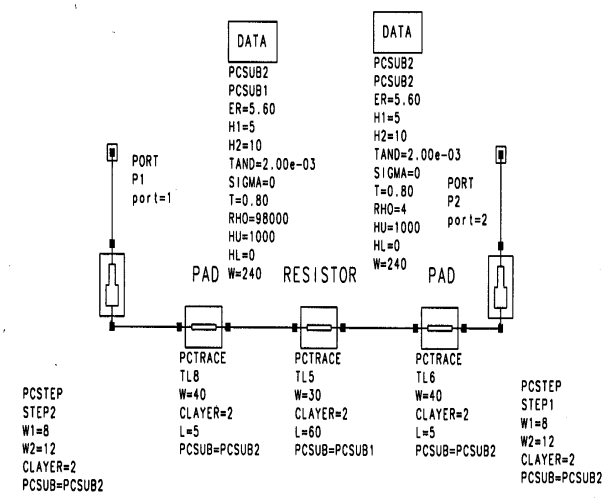

Figure 4 Resistor Model

INDUCTORS

The HP library model for square spiral inductors has been validated experimentally [2]. This model takes into account the mutual-inductive-coupling to all other parallel segments, including those of an image spiral, to account for the effect of the ground plane. The effect of the underpass is also taken into consideration [2].

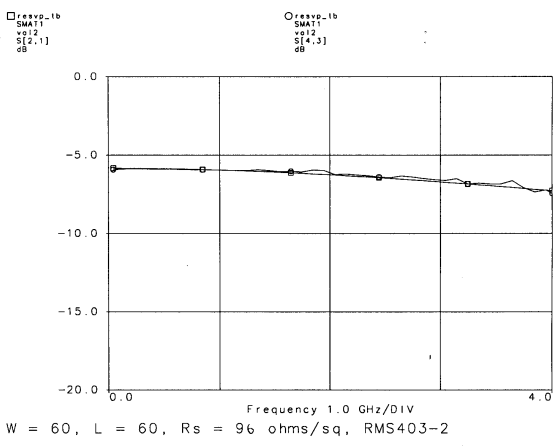

Figure 5 Validation of resistor's model. Measured results are represented by □ .The circuit model is represented by ○ .

Spiral inductors have been fabricated using 8-mil and 4-mil lines and spaces on a 15-mil substrate, where a maximum inductance of 90 nH was achieved with 260-mil square spiral. The measured S-parameters of various inductors are shown in Fig. 6. Very good agreement between measured and modeled results was obtained up to frequencies very close to the self-resonant frequency of these inductors. A peak Q value of 40 at 1.32 GHz for a 4.8 nH 8-mil spiral inductor was obtained, which is quite acceptable. Sarnoff is currently developing other LTCC-M processing techniques to further increase these Q values.

CONCLUSIONS

We have described our development of CAD models for lumped element resistors, capacitors and inductors. The CAD models were verified both experimentally and through complete EM field analysis. The developed semi-distributed circuit models are accurate and scaleable and have been incorporated into an LTCC-M design kit that interfaces with the standard, commercially-available HP Communication Design Suite software package [2].

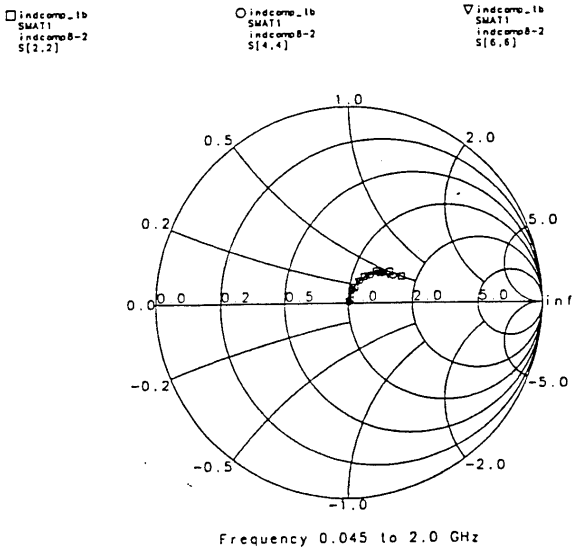

Figure 6 Validation of the inductor's model. Measured results from 2 different boards are represented by □ and ○ . The circuit model is represented by ▽.

LTCC-M technology allows accurate placement of passive embedded components such as resistors, capacitors, and resistors. This enables further miniaturization, and development of compact, reliable, low cost, 3D circuit integration technology.

ACKNOWLEDGMENTS

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REFERENCES

1) A. H. Kumar, A. N. Prabhu, B. J. Thaler, " Versatile, low cost, multilayer ceramic board on metal core," Proceedings of Int. Conf. on Multi-Chip Modules '95, p 100-107.

2) HP-Communication Design Suite, Series IV.

3) EM, and XGEOM, Sonnet Software Inc., Liverpool, NY.